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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/543,097	07/22/2005	Keiichi Kurashina	2005_1121A	5697

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EXAMINER	
LEADER, WILLIAM T	

ART UNIT	PAPER NUMBER
1723	

NOTIFICATION DATE	DELIVERY MODE
04/05/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/543,097	KURASHINA ET AL.	
	Examiner	Art Unit	
	WILLIAM T. LEADER	1723	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34,35 and 37-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34,35 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 24, 2011, has been entered.

2. Claims 34, 35 and 37-40 are pending.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Response to Amendment

4. The amendment to independent claim 34 is deemed to have overcome the rejection of record under 35 U.S.C. 102, and the rejections of record under 35 U.S.C. 103. The following new rejections are made.

Claim Rejections - 35 USC § 103

5. Claims 34, 35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos et al (US patent 6,773,570) in view of Chadda (US patent 7,025,860) or Emesh et al (US publication 2002/0108861) and additionally in view of Taylor et al (US patent 6,878,259) or Aylward (US patent 3,616,286), both newly cited.

6. As indicated in the previous office actions, the Economikos et al patent (hereinafter Economikos) is directed to a process for plating and planarizing a workpiece such as a semiconductor wafer (abstract, column 1, lines 11-23). The wafer 1 is illustrated in figure 1B and has a fine recess 3 for interconnects and is covered with a seed layer 4. .This corresponds to the first step of applicant's claim 34. As shown in figure 2, wafer 1 is mounted on carrier 12 and positioned opposite polishing pad 20. Polishing pad 20 is formed with holes 210 and 220 and is placed on table 10 (column 3, lines 63-65). Plating anodes 201, 202, 203, which are preferably sleeves of electrically conducting material, are placed in the holes (column 3, line 66 to column 7, line 3). Plating solution is pumped from reservoir 200 through the sleeves into the region between the anodes and seed layer 4 on wafer 1. This corresponds to the second step recited in instant claim 34. As in the third step of instant claim 34, the anodes of Economikos are connected to plating voltage source 250 and plating solution is continuously dispensed on pad 20 while the wafer rotates with respect to the pad (column 4, lines 9-22).

7. As shown in figure 6 and described at column 2, lines 65-67 of Economikos, electroplating and electroetching may be alternately performed a number of times. In electroplating a plating voltage is applied. In electroetching, a plating voltage is not applied. Economikos additionally discloses that during electroplating, a first amount of mechanical force is applied on the substrate against the pad (column 2, lines 57-61). During electroetching, the downward force on the wafer is reduced to allow a space greater than the boundary layer thickness to be formed (column 5, lines 8-12). This disclosure meets the limitation requiring a change of pressing state that is correlated with the change of state of plating voltage.

Economikos further discloses that the same solution used in the plating process may be used in the etching process (column 5, lines 3-8)

8. As previously indicated Economikos utilizes polishing pad 20 (column 3, lines 63-65) in the process of electroplating onto the seed layer of a semiconductor workpiece. While one of ordinary skill in the art would recognize that polishing pads have a degree of porosity, Economikos does not explicitly state that the polishing pad is porous. However, the porosity of such a pad is conventional as shown by Chadda or Emesh.

9. The Chadda patent is directed to a process for the electrochemical deposition and removal of a material on a workpiece surface. See the title and abstract. The workpiece may be a semiconductor wafer (column 1, lines 8-10). Chadda discloses that polishing pads may be made of blown urethane, which contains a large number of voids, or other material such as fiber meshes of felts which are porous (column 3, lines 28-40).

10. The Emesh patent is directed to a method for electrochemical treatment of a workpiece such as a semiconductor wafer (abstract; paragraph [0002]). As shown in figure 4, wafer 60 with a metalized surface 80 is urged against polishing pad 40 by wafer carrier assembly 130 (paragraph [0035]). The polishing pad may be formed from blown polyurethane (paragraph [0044]). A porous polishing pad facilitates transportation of the electrolytic solution to the wafer (paragraph 0045]).

11. Claim 34 as amended recites that plating is intermittently stopped by applying no voltage between the seed layer and anode for supplying plating solution between the seed layer and porous contact member. The Taylor et al patent (hereinafter Taylor) is directed to electrodeposition for metallization and planarization of semiconductor substrates. A metal such

as copper is electrodeposited into microscopic recesses to form electrical interconnects. See column 1, lines 20-47. In the process of Taylor, electric current in which cathodic pulses alternate with anodic pulses is utilized (column 2, lines 35-42). The current is illustrated in figure 1 which shows that rather than switching directly from cathodic to anodic polarity, off periods are provided between cathodic and anodic pulses. Taylor explains that when a metal is deposited onto a surface, the concentration of metal ions in the solution adjacent to the surface decreases. When pulsed current is used to effect metal deposition, the layer of solution adjacent to the surface can be at least partially replenished by diffusion during the periods when the cathodic (deposition) current is not flowing, specifically during the off-time and the anodic times. See column 9, line 42 to column 10, line 33.

12. The Aylward et al patent (hereinafter Aylward) is directed to electroplating a metal onto the internal surfaces of a porous structure. Conventional electroplating produces a deposit predominantly on the external surface instead of within the pores (column 1, lines 71-75). Aylward recognizes that the initial application of plating potential to the structure causes local depletion of the ions in the solution within the pores. To overcome this problem, Aylward teaches that when the ions are exhausted, the application of potential is stopped while fresh plating solution is supplied. Once the ions are replenished, a new plating cycle is carried out. See the abstract.

13. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have carried out the process of Economikos using a pad which was porous since this is conventional as shown by Chadda or Emesh, and to have included a period of time between the cathodic and anodic current pulses

when no voltage was applied because ions of the metal being deposited would have been replenished in the layer of solution adjacent to the surface being plated as taught by Taylor or Aylward.

14. With respect to claim 35, the change of pressing state is a change in downward force which results in a change in pressure (pressure = force per unit area).

15. With respect to claim 37, when the plating voltage is applied the pressure is relatively increased, and when the plating voltage is not applied the pressure is relatively lowered.

16. With respect to claim 38, the change in the pressing state in Economikos may be between contact and non-contact.

17. With respect to claim 39, the changes in pressure and voltage are synchronized to apply high pressure during application of the plating voltage.

18. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos et al (US patent 6,773,570) in view of Chadda (US patent 7,025,860) or Emesh et al (US publication 2002/0108861) and additionally in view of Taylor et al (US patent 6,878,259) or Aylward (US patent 3,616,286) as applied to claims 34, 35 and 37-39 above, and further in view of Matsuda et al (US 6,375,823).

19. Claim 40 additionally recites applying plating voltage after a period of time after the porous contact member is brought into contact with the surface of the seed layer. Economikos is silent as to the sequence of contacting and applying a voltage. The Matsuda et al patent (hereinafter Matsuda) is directed to a method for plating onto a workpiece such as a semiconductor device (abstract, column 1, lines 12-14). The workpiece is shown in figure 2 and

has fine recesses and conductive layer 103 which includes a copper seed layer (column 9, lines 50-56). A pad 111 is dipped into a plating bath to impregnate the pad with plating solution (column 10, lines 15-18). The pad is made of a porous material (column 10, lines 3-7). Matsuda discloses that the impregnated pad is brought into tight contact with the seed layer and then a plating current is applied (column 10, lines 26-31). It would have been obvious to have utilized the sequence disclosed by Matsuda in the process of Economikos because plating would not have commenced until the desired orientation of the parts was obtained.

Response to Arguments

20. Applicant's arguments with respect to claims 34, 35 and 37-40 as amended have been considered but are moot in view of the new ground(s) of rejection.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Mentone patent is directed to a process for electroplating a metal onto small conductors. Mentone discloses that under continuous plating conditions, the solution immediately adjoining the conductors is normally depleted of plating ions rather quickly so that the continuing application of current achieves less efficient plating. Mentone teaches the application of current in intermittent pulses. When the pulse is terminated and a rest period is provided, the plating solution can replenish ions in the immediate vicinity of the conductor. See column 1, lines 40-61.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM T. LEADER whose telephone number is (571) 272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa D. Neckel can be reached on 571-272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William Leader/
March 25, 2011

/Alexa D. Neckel/
Supervisory Patent Examiner, Art Unit 1723